

**In the Claims:**

1.-16. (Canceled)

17. (Currently Amended) A method of fabricating a capacitor of a semiconductor device, the method comprising:

forming a capacitor lower electrode on a semiconductor substrate;

forming a dielectric layer on the lower electrode; and

sequentially stacking a metallic layer and a polySi<sub>1-x</sub>Ge<sub>x</sub> layer on the dielectric layer to form an upper electrode comprising the metallic layer and the polySi<sub>1-x</sub>Ge<sub>x</sub> layer, wherein the polySi<sub>1-x</sub>Ge<sub>x</sub> layer is formed at about 550°C or less.

18. (Previously Presented) The method of Claim 17 wherein the polySi<sub>1-x</sub>Ge<sub>x</sub> layer comprises a doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer.

19. (Original) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is formed by doping a polySi<sub>1-x</sub>Ge<sub>x</sub> layer with P or As.

20. (Original) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is formed by doping a polySi<sub>1-x</sub>Ge<sub>x</sub> layer with B.

21. (Original) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is formed by depositing a polySi<sub>1-x</sub>Ge<sub>x</sub> layer while simultaneously doping impurities.

22. (Original) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is deposited and simultaneously activated.

23. (Previously Presented) The method of Claim 22, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> is deposited and simultaneously activated between about 350°C and about 550°C.

24. (Original) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is deposited and then activation and thermal treatment is performed.

25. (Original) The method of Claim 24, wherein activation and thermal treatment is performed between about 400°C and about 550°C.

26. (Original) The method of Claim 17, wherein the metallic layer of the upper electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof.

27. (Previously Presented) The method of Claim 18, wherein the doped polySi<sub>1-x</sub>Ge<sub>x</sub> layer is formed using low pressure chemical vapor deposition (LP CVD) using furnace type equipment, single wafer type equipment, and/or mini-batch equipment.

28. (Original) The method of Claim 17, wherein the lower electrode comprises a metallic layer.

29. (Original) A method of fabricating a capacitor of a semiconductor device, the method comprising:

- forming a capacitor lower electrode on a semiconductor substrate;
- forming a dielectric layer on the lower electrode; and
- forming an Si<sub>1-x</sub>Ge<sub>x</sub> layer on the dielectric layer at about 550°C or less.

30. (Original) A method according to Claim 29, further comprising:  
thermally treating the Si<sub>1-x</sub>Ge<sub>x</sub> layer at about 550°C or less.

31. (Previously Presented) A method according to Claim 29 wherein the following is performed between forming a dielectric layer and forming an Si<sub>1-x</sub>Ge<sub>x</sub> layer:

- forming a metallic layer on the dielectric layer; and

wherein forming an  $\text{Si}_{1-x}\text{Ge}_x$  layer comprises forming an  $\text{Si}_{1-x}\text{Ge}_x$  layer on the metallic layer at about 550°C or less.

32. (Previously Presented) A method according to Claim 29 wherein the  $\text{Si}_{1-x}\text{Ge}_x$  layer comprises a poly $\text{Si}_{1-x}\text{Ge}_x$  layer.

33. (Canceled)

34. (Previously Presented) A method according to Claim 29 wherein the lower electrode comprises a metallic layer.

35. (New) The method of Claim 17 wherein x is between 0.1 and 0.9.

36. (New) The method of Claim 17 wherein x is between 0.1 and 0.6.

37. (New) A method according to Claim 29 wherein x is between 0.1 and 0.9.

38. (New) A method according to Claim 29 wherein x is between 0.1 and 0.6.